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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/505,216	08/20/2004	Shinya Miyazaki	501.43896X00	2389

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/505,216	MIYAZAKI ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/20/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Pre-amendment filed on 8/20 2004 has been entered.

2. Pre-amendment filed on 11/08/ 2004 has been entered.

3. Claims 16-31 have been canceled.

4. Claims 1-15 are presented for examination.

Information Disclosure Statement

5. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 08/20/2004.

6. Information disclosed and list on PTO 1449 was considered.

Specification

7. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Jung (U.S. Patent No. 6,034,884).

Regarding claims 1-15, Jung discloses a semiconductor integrated circuit (Figure 3) having over one semiconductor substrate a nonvolatile memory (102) and a logic circuit (Column 2, lines 13-20) which uses information stored in said nonvolatile memory to perform logical operation (Column 3, lines 51-65),

wherein said nonvolatile memory comprises bit lines (BLn, BNnB), word lines (WL), and memory cells(MC),

wherein said memory cell comprises a MOS transistor (T1) whose gate electrode is connected with a word line (WL1), and information storage is carried out according to whether one source/drain electrode of said MOS transistor is connected with a current path or floated (Column 3, lines 1-6) ,

and wherein a control circuit (104) is provided which produces a potential difference between the source/drain electrodes of said MOS transistor during a predetermined period in the operation of accessing said memory cell (Column 2, lines 1-23), and makes zero the potential difference between the source/drain electrodes of said MOS transistor during the other periods than said predetermined period (Column3, lines 1-22, Figures 2A-2B).

More specifically, Jung discloses wherein the time at which a potential difference is produced between the source/drain electrodes of said MOS transistor is matched with or behind the time at which a word line is selected (Column 3, lines 14-22), and the nonvolatile memory and logic circuit use common supply voltage (Figure 1) and as their operating power supply voltage

(Figure 3), and wherein whether a MOS transistor is connected with said current path or floated is determined according to whether the one source/drain electrode thereof on the opposite side to the bit line is connected with a predetermined signal line or not (Figure 3, Column 3, lines 23-36), and wherein one memory cell has two MOS transistors (Figure 3, T1, T2), and the other source/drain electrodes of the two MOS transistors are connected constitute complementary bit lines (BLnB) with separate bit lines (BLn) which bit lines and the gate electrodes of the two MOS transistors are connected with a common word line (WL1), and further comprising an amplifier which amplifies the potential difference between said complementary bit lines (Figure 3, 108).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER